

Example of reading instruction set tables. ADC A...ADC A - entry says to see table; table shows opcode 8F, 4 states, and flag code 'A' which is defined under 'Flag Codes'.
ADC HL BC...2 byte opcode is ED, 4A, flag code is H, takes 15 states. CALL C, address...opcode is DC followed by 2 byte address; flag code is Z, states are described by note 5.

Instruction Set

A	ADC A...	A...	LD (IX+d), C	Z19
	ADC HL, BC	H15	LD (IX+d), D	Z19
	ADC HL, DE	H15	LD (IX+d), E	Z19
	ADC HL, HL	H15	LD (IX+d), H	Z19
	ADC HL, SP	H15	LD (IX+d), L	Z19
	ADD A...	A	LD (IX+d), A	Z19
	ADD HL, BC	G11	LD (IX+d), B	Z19
	ADD HL, DE	G11	LD (IX+d), C	Z19
	ADD HL, HL	G11	LD (IX+d), D	Z19
	ADD HL, SP	G11	LD (IX+d), E	Z19
	ADD IX, BC	G15	LD (IX+d), H	Z19
	ADD IX, DE	G15	LD (IX+d), L	Z19
	ADD IX, IX	G15	LD (aa), A	Z13
	ADD IX, SP	G15	LD (aa), BC	Z20
	ADD IY, BC	G15	LD (aa), DE	Z20
	ADD IY, DE	G15	LD (aa), HL	Z20
	ADD IY, IY	G15	LD (aa), IX	Z20
	ADD IY, SP	G15	LD (aa), SP	Z20
	AND ...	C	LD A, (BC)	Z7
	CALL ...	Z17	LD A, (DE)	Z13
	CALL C, aa	Z(5)	LD A, I	U9
	CALL M, aa	Z(5)	LD B...	Z
	CALL NC, aa	Z(5)	LD BC, (aa)	Z20
	CALL NZ, aa	Z(5)	LD BC, aa	Z10
	CALL P, aa	Z(5)	LD D...	Z
	CALL PE, aa	Z(5)	LD D, A	Z
	CALL PO, aa	Z(5)	LD D, B	Z
	CALL Z, aa	Z(5)	LD D, C	Z
	CP ...	B	LD D, D	Z
	CPD ...	T16	LD D, E	Z
	CPDR ...	T(1)	LD D, (aa)	Z20
	CPI ...	T16	LD D, DE, aa	Z10
	CPIC ...	T(1)	LD D, E	Z
	CPL ...	N4	LD D, H	Z
	DAA ...	M4	LD D, HL, (aa)	Z16
	DEC (HL)	F11	LD D, HL, aa	Z10
	DEC (IX+d)	F23	LD D, LA	Z
	DEC (IX+d)	F23	LD D, IX, (aa)	Z20
	DEC A	F4	LD D, IX, aa	Z14
	DEC B	F4	LD D, IY, (aa)	Z20
	DEC BC	F4	LD D, IY, aa	Z14
	DEC C	F4	LD D, L	Z
	DEC D	F4	LD D, R, A	Z9
	DEC DE	F4	LD D, SP, (aa)	Z20
	DEC E	F4	LD D, SP, HL	Z6
	DEC H	F4	LD D, SP, IX	Z10
	DEC HL	F4	LD D, SP, IY	Z10
	DEC IY	Z10	LD D, SP, aa	Z10
	DEC IY	Z10	LD D, LDDR	R16
	DEC L	F4	LDI	S(1)
	DEC SP	Z4	LDIR	R16
	DI	Z4	LDI	S(1)
	DJNZ d	Z(2)	NEG	BB
	EI	Z4	NOP	Z4
	EX (SP), HL	Z19	OR	Q(1)
	EX (SP), IX	Z23	OTDR	Q(1)
	EX (SP), IY	Z23	OTIR	Q(1)
	EX AF, AF	Z4	OUT (C), A	Z12
	EX DE, HL	Z4	OUT (C), B	Z12
	EXX	Z4	OUT (C), C	Z12
	HALT	Z4	OUT (C), D	Z12
	IM 0	Z8	OUT (C), E	Z12
	IM 1	Z8	OUT (C), H	Z12
	IM 2	Z8	OUT (C), L	Z12
	IN A, (C)	W12	OUT (C), A	Z11
	IN A, (n)	Z11	OUT (C), L	Z11
	IN B, (C)	W12	OUTD	P16
	IN C, (C)	W12	OUTI	P16
	IN D, (C)	W12	POP AF	Z10
	IN E, (C)	W12	POP BC	Z10
	IN H, (C)	W12	POP DE	Z10
	IN L, (C)	W12	POP HL	Z10
	INC (HL)	E11	POP IX	Z14
	INC (IX+d)	E23	POP IY	Z11
	INC (IX+d)	E23	PUSH AF	Z11
	INC A	E4	PUSH BC	Z11
	INC B	E4	PUSH DE	Z11
	INC BC	E4	PUSH HL	Z11
	INC C	E4	PUSH IX	Z15
	INC D	E4	PUSH IY	Z15
	INC DE	E4	PUSH	Z15
	INC E	E4	RES	Z10
	INC H	E4	RET	Z(4)
	INC HL	Z10	RET C	Z(4)
	INC IX	Z10	RET M	Z(4)
	INC IY	Z10	RET NC	Z(4)
	INC L	E4	RET NZ	Z(4)
	INC SP	E4	RET P	Z(4)
	IND	P16	RET PE	Z(4)
	INDR	Q(1)	RET PO	Z(4)
	INIR	Q(1)	RET Z	Z(4)
	JP (HL)	Z10	RETI	Z14
	JP (IX)	Z8	RETN	Z14
	JP (IY)	Z8	RL	K
	JP aa	Z10	RLA	J4
	JP C, aa	Z10	RLC	K
	JP M, aa	Z10	RLCA	J4
	JP NC, aa	Z10	RLD	L18
	JP NZ, aa	Z10	RR	K
	JP PE, aa	Z10	RRA	K
	JP PO, aa	Z10	RRC	J4
	JP Z, aa	Z10	RRCA	K
	JR C, d	Z(3)	RRD	L18
	JR d	Z12	RST 00H	Z11
	JR NC, d	Z(3)	RST 08H	Z11
	JR NZ, d	Z(3)	RST 10H	Z11
	JR Z, d	Z(3)	RST 18H	Z11
	LD (BC), A	Z7	RST 20H	Z11
	LD (DE), A	Z7	RST 28H	Z11
	LD (HL), A	Z7	RST 30H	Z11
	LD (HL), B	Z7	RST 38H	Z11
	LD (HL), C	Z7	SBC HL, BC	I15
	LD (HL), D	Z7	SBC HL, DE	I15
	LD (HL), E	Z7	SBC HL, HL	I15
	LD (HL), H	Z7	SBC HL, SP	I15
	LD (HL), L	Z7	SCF	O4
	LD (HL), n	Z10	SET	Z
	LD (IX+d), A	Z19	SLA	K
	LD (IX+d), B	Z19	SRA	K
	LD (IX+d), C	Z19	SRL	K
	LD (IX+d), D	Z19	SUB	B
	LD (IX+d), E	Z19	XOR	B

	A	B	C	D	E	H	L	(HL)	(IX+d)	(IY+d)		
BIT 0	CB.4F	CB.40	CB.41	CB.42	CB.43	CB.44	CB.45	CB.46	DD, CB.d.46	FD, CB.d.46	V	
BIT 1	CB.4F	CB.48	CB.49	CB.4A	CB.4B	CB.4C	CB.4D	CB.4E	DD, CB.d.4E	FD, CB.d.4E	V	
BIT 2	CB.57	CB.50	CB.51	CB.52	CB.53	CB.54	CB.55	CB.56	DD, CB.d.56	FD, CB.d.56	V	
BIT 3	CB.5F	CB.58	CB.59	CB.5A	CB.5B	CB.5C	CB.5D	CB.5E	DD, CB.d.5E	FD, CB.d.5E	V	
BIT 4	CB.67	CB.60	CB.61	CB.62	CB.63	CB.64	CB.65	CB.66	DD, CB.d.66	FD, CB.d.66	V	
BIT 5	CB.6F	CB.68	CB.69	CB.6A	CB.6B	CB.6C	CB.6D	CB.6E	DD, CB.d.6E	FD, CB.d.6E	V	
BIT 6	CB.77	CB.70	CB.71	CB.72	CB.73	CB.74	CB.75	CB.76	DD, CB.d.76	FD, CB.d.76	V	
BIT 7	CB.7F	CB.78	CB.79	CB.7A	CB.7B	CB.7C	CB.7D	CB.7E	DD, CB.d.7E	FD, CB.d.7E	V	
STATES:	8				12				20			

	A	B	C	D	E	H	L	(HL)	(IX+d)	(IY+d)		
RES 0	CB.87	CB.80	CB.81	CB.82	CB.83	CB.84	CB.85	CB.86	DD, CB.d.86	FD, CB.d.86	Z	
RES 1	CB.8F	CB.88	CB.89	CB.8A	CB.8B	CB.8C	CB.8D	CB.8E	DD, CB.d.8E	FD, CB.d.8E	Z	
RES 2	CB.97	CB.90	CB.91	CB.92	CB.93	CB.94	CB.95	CB.96	DD, CB.d.96	FD, CB.d.96	Z	
RES 3	CB.9F	CB.98	CB.99	CB.9A	CB.9B	CB.9C	CB.9D	CB.9E	DD, CB.d.9E	FD, CB.d.9E	Z	
RES 4	CB.A7	CB.A0	CB.A1	CB.A2	CB.A3	CB.A4	CB.A5	CB.A6	DD, CB.d.A6	FD, CB.d.A6	Z	
RES 5	CB.AF	CB.A8	CB.A9	CB.AA	CB.AB	CB.AC	CB.AD	CB.AE	DD, CB.d.AE	FD, CB.d.AE	Z	
RES 6	CB.B7	CB.B0	CB.B1	CB.B2	CB.B3	CB.B4	CB.B5	CB.B6	DD, CB.d.B6	FD, CB.d.B6	Z	
RES 7	CB.BF	CB.B8	CB.B9	CB.BA	CB.BB	CB.BC	CB.BD	CB.BE	DD, CB.d.BE	FD, CB.d.BE	Z	
SET 0	CB.C7	CB.C0	CB.C1	CB.C2	CB.C3	CB.C4	CB.C5	CB.C6	DD, CB.d.C6	FD, CB.d.C6	Z	
SET 1	CB.CF	CB.C8	CB.C9	CB.CA	CB.CB	CB.CC	CB.CD	CB.CE	DD, CB.d.CE	FD, CB.d.CE	Z	
SET 2	CB.D7	CB.D0	CB.D1	CB.D2	CB.D3	CB.D4	CB.D5	CB.D6	DD, CB.d.D6	FD, CB.d.D6	Z	
SET 3	CB.DF	CB.D8	CB.D9	CB.DA	CB.DB	CB.DC	CB.DD	CB.DE	DD, CB.d.DE	FD, CB.d.DE	Z	
SET 4	CB.E7	CB.E0	CB.E1	CB.E2	CB.E3	CB.E4	CB.E5	CB.E6	DD, CB.d.E6	FD, CB.d.E6	Z	
SET 5	CB.EF	CB.E8	CB.E9	CB.EA	CB.EB	CB.EC	CB.ED	CB.EE	DD, CB.d.EE	FD, CB.d.EE	Z	
SET 6	CB.F7	CB.F0	CB.F1	CB.F2	CB.F3	CB.F4	CB.F5	CB.F6	DD, CB.d.F6	FD, CB.d.F6	Z	
SET 7	CB.FF	CB.F8	CB.F9	CB.FA	CB.FB	CB.FC	CB.FD	CB.FE	DD, CB.d.FE	FD, CB.d.FE	Z	
STATES:	8				15				23			

	A(8)	B	C	D	E	H	L	(HL)	(IX+d)	(IY+d)		
RLC	CB.07	CB.00	CB.01	CB.02	CB.03	CB.04	CB.05	CB.06	DD, CB.d.06	FD, CB.d.06	K	
RRC	CB.0F	CB.08	CB.09	CB.0A	CB.0B	CB.0C	CB.0D	CB.0E	DD, CB.d.0E	FD, CB.d.0E	K	
RL	CB.17	CB.10	CB.11	CB.12	CB.13	CB.14	CB.15	CB.16	DD, CB.d.16	FD, CB.d.16	K	
RR	CB.1F	CB.18	CB.19	CB.1A	CB.1B	CB.1C	CB.1D	CB.1E	DD, CB.d.1E	FD, CB.d.1E	K	
SLA	CB.27	CB.20	CB.21	CB.22	CB.23	CB.24	CB.25	CB.26	DD, CB.d.26	FD, CB.d.26	K	
SRA	CB.2F	CB.28	CB.29	CB.2A	CB.2B	CB.2C	CB.2D	CB.2E	DD, CB.d.2E	FD, CB.d.2E	K	
SRL	CB.3F	CB.38	CB.39	CB.3A	CB.3B	CB.3C	CB.3D	CB.3E	DD, CB.d.3E	FD, CB.d.3E	K	
STATES:	8				15				23			

Flag Codes

	C	Z	P	V	S	N	H
A	1	1	1	1	1	1	1
B	1	1	1	1	1	1	1
C	1	1	1	1	1	1	1
D	1	1	1	1	1	1	1
E	1	1	1	1	1	1	1
F	1	1	1	1	1	1	1
G	1	1	1	1	1	1	1
H	1	1	1	1	1	1	1
I	1	1	1	1	1	1	1
J	1	1	1	1	1	1	1
K	1	1	1	1	1	1	1
L	1	1	1	1	1	1	1
M	1	1	1	1	1	1	1
N	1	1	1	1	1	1	1
O	1	1	1	1	1	1	1
P	1	1	1	1	1	1	1
Q	1	1	1	1	1	1	1
R	1	1	1	1	1	1	1
S	1	1	1	1	1	1	1
T	1	1	1	1	1	1	1
U	1	1	1	1	1	1	1
V	1	1	1	1	1	1	1
W	1	1	1	1	1	1	1
X	1	1	1	1	1	1	1
Y	1	1	1	1	1	1	1
Z	1	1	1	1	1	1	1

Codes:
0: reset
1: set
C: Carry*
F: Footnote
H: Half carry*
N: Add/Sub*
P: Parity*
S: Sign*
U: Undefined
V: overflow*
Z: Zero*
=: not affected

* Indicated flag affected by result

(1) Z=1 iff B becomes 0
(2) PV=0 iff BC becomes 0
(3) PV=0 iff BC becomes 0 and Z=1 iff A=(HL)
(4) PV=IFF2
(5) Z=5iff

LSD →

Single-Byte-Opcode to Instruction Conversion

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	NOP	LD BC,nn	LD (BC),A	INC BC	INC B	DEC B	LD B,n	RLCA	EX AF,AF	ADD HL,BC	LD A,(BC)	DEC BC	INC C	DEC C	LD C,n	RRCA
1	DJNZ n	LD DE,nn	LD (DE),A	INC DE	INC D	DEC D	LD D,n	RLA	JR n	ADD HL,DE	LD A,(DE)	DEC DE	INC E	DEC E	LD E,n	RRA
2	JR NZ,n	LD HL,nn	LD (HL),HL	INC HL	INC H	DEC H	LD H,n	DAA	JR Z,n	ADD HL,HL	LD L,(nn)	DEC HL	INC L	DEC L	LD L,n	CPL
3	JR NC,n	LD SP,nn	LD (nn),A	INC SP	INC (HL)	DEC (HL)	LD (HL),n	SCF	JR C,n	ADD HL,SP	LD A,(nn)	DEC SP	INC A	DEC A	LD A,n	CF
4	LD B,B	LD B,C	LD B,D	LD B,E	LD B,H	LD B,L	LD B,(HL)	LD B,A	LD C,B	LD C,C	LD C,D	LD C,E	LD C,H	LD C,L	LD C,(HL)	LD C,A
5	LD D,B	LD D,C	LD D,D	LD D,E	LD D,H	LD D,L	LD D,(HL)	LD D,A	LD E,B	LD E,C	LD E,D	LD E,E	LD E,H	LD E,L	LD E,(HL)	LD E,A
6	LD H,B	LD H,C	LD H,D	LD H,E	LD H,H	LD H,L	LD H,(HL)	LD H,A	LD L,B	LD L,C	LD L,D	LD L,E	LD L,H	LD L,L	LD L,(HL)	LD L,A
7	LD (HL),B	LD (HL),C	LD (HL),D	LD (HL),E	LD (HL),H	LD (HL),L	HALT	LD (HL),A	LD A,B	LD A,C	LD A,D	LD A,E	LD A,H	LD A,L	LD A,(HL)	LD A,A
8	ADD A,B	ADD A,C	ADD A,D	ADD A,E	ADD A,H	ADD A,L	ADD A,(HL)	ADD A,A	ADC A,B	ADC A,C	ADC A,D	ADC A,E	ADC A,H	ADC A,L	ADC A,(HL)	ADC A,A
9	SUB B	SUB C	SUB D	SUB E	SUB H	SUB L	SUB (HL)	SUB A	SBC A,B	SBC A,C	SBC A,D	SBC A,E	SBC A,H	SBC A,L	SBC A,(HL)	SBC A,A
A	AND B	AND C	AND D	AND E	AND H	AND L	AND (HL)	AND A	XOR B	XOR C	XOR D	XOR E	XOR H	XOR L	XOR (HL)	XOR A
B	OR B	OR C	OR D	OR E	OR H	OR L	OR (HL)	OR A	CP B	CP C	CP D	CP E	CP H	CP L	CP (HL)	CP A
C	RET NZ	POP BC	JP NZ,nn	JP nn	CALL NZ,nn	PUSH BC	ADD n	RST 00H	RET Z	RET	JP Z,nn	table	CALL Z,nn	CALL nn	ADC A,n	RST 00H
D	RET NC	POP DE	JP NC,nn	JP (n),A	CALL NC,nn	PUSH DE	SUB n	RST 10H	RET C	EXX	JP C,nn	IN A,(n)	CALL C,nn	table	SBC A,n	RST 10H
E	RET PO	POP HL	JP PO,nn	DI (SP),HL	CALL PO,nn	PUSH HL	AND n	RST 20H	RET PE	JP (HL)	JP PE,nn	EX DE,HL	CALL PE,nn	table	XOR n	RST 20H
F	RET P	POP AF	JP P,nn	EX	CALL P,nn	PUSH AF	OR n	RST 30H	RET M	LD SP,HL	JP M,nn	EI	CALL M,nn	table	CP n	RST 30H

Multi-Byte-Opcode to Instruction Conversion

CB00	RLC B	ED40	IN B,(C)	%09	ADD XY,BC	%CBd06	RLC (XY+d)
CB01	RLC C	ED41	OUT (C),B	%19	ADD XY,DE	%CBd0E	RRC (XY+d)
CB02	RLC D	ED42	SBC HL,BC	%21aa	LD Y,aa	%CBd16	RL (XY+d)
CB03	RLC E	ED43aa	LD (aa),BC	%22aa	LD (aa),XY	%CBd1E	RR (XY+d)
CB04	RLC H	ED44	NEG	%23	INC XY	%CBd26	SLA (XY+d)
CB05	RLC L	ED45	RETN	%29	ADD XY,XY	%CBd2E	SRA (XY+d)
CB06	RLC (HL)	ED46	IM 0	%2Aaa	LD XY,(aa)	%CBd3E	SRL (XY+d)
CB07	RLCA	ED47	LD I,A	%2B	DEC XY	%CBd46	BIT 0,(XY+d)
CB08	RRC B	ED48	IN C,(C)	%34ad	INC (XY+d)	%CBd4E	BIT 1,(XY+d)
CB09	RRC C	ED49	OUT (C),C	%35d	DEC (XY+d)	%CBd56	BIT 2,(XY+d)
CB0A	RRC D	ED4A	ADC HL,BC	%36dn	LD (XY+d),n	%CBd5E	BIT 3,(XY+d)
CB0B	RRC E	ED4Baa	LD BC,(aa)	%39	ADD XY,SP	%CBd66	BIT 4,(XY+d)
CB0C	RRC H	ED4D	RETI	%46d	LD B,(XY+d)	%CBd6E	BIT 5,(XY+d)
CB0D	RRC L	ED4F	LD R,A	%4Ed	LD C,(XY+d)	%CBd76	BIT 6,(XY+d)
CB0E	RRC (HL)	ED50	IN D,(C)	%56d	LD D,(XY+d)	%CBd86	RES 0,(XY+d)
CB0F	RRC A	ED51	OUT (C),D	%5Ed	LD E,(XY+d)	%CBd8E	RES 1,(XY+d)
CB10	RL B	ED52	SBC HL,DE	%66d	LD A,(XY+d)	%CBd9E	RES 2,(XY+d)
CB11	RL C	ED53aa	LD (aa),DE	%6Ed	LD L,(XY+d)	%CBdA6	RES 3,(XY+d)
CB12	RL D	ED56	IM 1	%70d	LD (XY+d),B	%CBdAE	RES 4,(XY+d)
CB13	RL E	ED57	LD A,I	%71d	LD (XY+d),C	%CBdB6	RES 5,(XY+d)
CB14	RL H	ED58	IN E,(C)	%72d	LD (XY+d),D	%CBdB6E	RES 6,(XY+d)
CB15	RL L	ED59	OUT (C),E	%73d	LD (XY+d),E	%CBdC6	RES 7,(XY+d)
CB16	RL (HL)	ED5A	ADC HL,DE	%74d	LD (XY+d),H	%CBdC6E	SET 0,(XY+d)
CB17	RL A	ED5Baa	LD DE,(aa)	%75d	LD (XY+d),L	%CBdD6	SET 1,(XY+d)
CB18	RR B	ED5E	IM 2	%77d	LD (XY+d),A	%CBdD6E	SET 2,(XY+d)
CB19	RR C	ED5F	LD A,R	%8Ed	ADD A,(XY+d)	%CBdE6	SET 3,(XY+d)
CB1A	RR D	ED60	IN H,(C)	%8Ed	ADC A,(XY+d)	%CBdE6E	SET 4,(XY+d)
CB1B	RR E	ED61	OUT (C),H	%96d	SUB (XY+d)	%CBdFE	SET 5,(XY+d)
CB1C	RR H	ED62	SBC HL,HL	%9Ed	SBC A,(XY+d)	%E1	POP XY
CB1D	RR L	ED67	RDD	%A6d	AND (XY+d)	%E3	EX (SP),XY
CB1E	RR (HL)	ED68	IN L,(C)	%AEd	XOR (XY+d)	%E9	PUSH XY
CB1F	RR A	ED69	OUT (C),L	%B6d	OR (XY+d)	%F9	JP (XY)
CB20	SLA B	ED6A	ADC HL,HL	%BEd	CP (XY+d)		LD SP,XY
CB21	SLA C	ED6F	RLD				
CB22	SLA D	ED72	SBC HL,SP				
CB23	SLA E	ED73aa	LD (aa),SP				
CB24	SLA H	ED78	IN A,(C)				
CB25	SLA L	ED79	OUT (C),A				
CB26	SLA (HL)	ED7A	ADC HL,SP				
CB27	SLA A	ED7Baa	LD SP,(aa)				
CB28	SRA B	EDA0	LDI				
CB29	SRA C	EDA1	CPI				
CB2A	SRA D	EDA2	INI				
CB2B	SRA E	EDA3	OUTI				
CB2C	SRA H	EDA8	LDD				
CB2D	SRA L	EDA9	CPD				
CB2E	SRA (HL)	EDAA	IND				
CB2F	SRA A	EDAB	OUTD				
CB30	SRL B	EDB0	LDIR				
CB31	SRL C	EDB1	ODIR				
CB32	SRL D	EDB2	INIR				
CB33	SRL E	EDB3	OTIR				
CB34	SRL H	EDB8	LDDR				
CB35	SRL L	EDB9	CPDR				
CB36	SRL (HL)	EDBA	INDR				
CB3F	SRL A	EDBB	OTDR				
CB40	see BIT						
CBFF	see RES						

%% means DD or FD and for DD, XY means IX for FD, XY means IY

Powers of Two

1	2	9	512
2	4	10	1,024
3	8	11	2,048
4	16	12	4,096
5	32	13	8,192
6	64	14	16,384
7	128	15	32,768
8	256	16	65,536
17	131,072		
18	262,144		
19	524,288		
20	1,048,576		
21	2,097,152		
22	4,194,304		
23	8,388,608		
24	16,777,216		

Unsigned Comparisons

example: CP B

A < B	JP C,YES
A ≤ B	JP C,YES
A = B	JP Z,YES
A ≥ B	JP N,C,YES
A > B	JP N,C,YES

YES represents label for code to be executed if condition is true. Internally, A-B is computed to determine flags as for 'SUB B'.

① Requires both instructions.

A11	1	40	A10
A12	2	39	A9
A13	3	38	A8
A14	4	37	A7
A15	5	36	A6
	6	35	A5
D4	7	34	A4
D3	8	33	A3
D6	9	32	A2
D5	10	31	A1
+V	11	30	A0
D2	12	29	GND
D7	13	28	RES
D0	14	27	MI
O1	15	26	RESET
NMI	16	25	SUSP
HALT	17	24	WAIT
MREQ	18	23	SUSAK
TORQ	19	22	MR
	20	21	RD

main	alternate	special	Registers
A	F	I	R
B	C	INDEX IX	
D	E	INDEX IY	
H	L	STCK PTR SP	
			small=8 bit large=16 bit PGRM CTR PC

Status Flags

MSB	LSB				
S	Z	H	P/V	N	C

S = Sign (MSB) of result
Z = 1 when result is Zero
H = Half carry from bit 3
P/V = 1 = Parity even for logic op or overflow for arithmetic op
N = 1 when last op was subtract (0 for add)
C = Carry (CY)

Interrupts and Reset

Falling edge sensitive NMI does a RST 66H regardless of IFF1, 2 (Interrupt Flip Flop).

If interrupts are enabled (IFF1=1), low level sensitive INT depends on mode:
MODE 0: Interrupting device puts instruction on bus (e.g. RST or CALL). Takes 2 extra time states.
MODE 1: Does a RST 30H (Z13).
MODE 2: Location pointed to by 15 87 10 and next hold vector of service subroutine, iv (7 bit int vector index) is put on data bus by interrupting device (Z19).

IFF1 and IFF2 are both cleared by INT or DI. Both are set by EI.
NMI clears IFF1. RETN loads IFF1 from IFF2. LD A,I and LD A,R set P/V flag to IFF2. Reset sets PC=0, IFF1=IFF2=0, I=0, R=0, MODE=0.

General Instruction Description (except shifts)

ADC x,y Add y+CY to x.
ADD y,x Add y to x.
AND x to A AND x to A.
BIT b,x Test bit b of x.
CALL x,x Call subroutine at x (push PC and jump to x).
CF Complement carry flag.
CP Compare A with x (see "Unsigned Comparisons").
CPD Compare A with (HL), DEC HL, DEC BC.
CPI Like CPD but repeat until A=(HL) or BC=0.
CPDR Compare A with (HL), INC HL, DEC BC.
CPIR Like CPI, but repeat until A=(HL) or BC=0.
CPL Complement A (1's comp.).
DAA Decimal adjust A (after add or sub of BCD data).
DEC x,y Decrement x by 1.
DI Disable interrupts.
DJNZ d,j Decrement B, jump relative by d if B not zero. Enable interrupts after next instruction.
EI Exchange with EI.
EXX Exchange BC, DE, HL with BC, DE: HL.
HALT Halt (wait for interrupt or reset).
IM x Set interrupt mode to x.
IN A,(n) Input port n into A (6).
IN r,(C) Input port (C) into r (7).
INC x,y Increment x by 1.
IND Load (HL) from port (C), DEC B, DEC HL (7). Like IND, but repeat until B=0 (7).
INIR Like INI, but repeat until B=0 (7).
JP c,x Jump to location x.
JP r,c Jump to location x if condition c is true jump relative by d.
JR d,j Jump relative by d.
LD x,y Load x with y (move y to x).
LDD Load (DE) with (HL), DEC DE, DEC HL, DEC BC.
LDDR Load LDD, but repeat until BC=0.
LDI Load (DE) with (HL), INC DE, INC HL, DEC BC.
LDIR Like LDI, but repeat until BC=0.
NEG Negate A (2's comp.).
NOP No operation.
OR x to A OR x to A.
OTDR Like OUTD, but repeat until B=0 (7).
OUTI Like OUTI, but repeat until B=0 (7).
OUT (C),r Output r to port (C) (7).
OUT (n),A Output (HL) to port (C), DEC B, DEC HL (7).
OUTD Output (HL) to port (C), DEC B, INC HL (7).
POP x Pop x from top of stack updating SP.
PUSH x Push x onto top of stack updating SP.
RES b of x (to 0).
RET Return from subroutine (pop PC).
RET c Return from subroutine if condition c is true return from subroutine.
RETI Return from interrupt.
RETN Return from NMI (see "Interrupts").
RST x Call subroutine at x (1 byte inst).
SBC x,y Subtract y+CY from x.
SCF Set carry flag (to 1).
SET b of x (to 1).
SUB x from A Subtract x from A.
XOR x to A XOR x to A.

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